AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A DC voltage generator system for supplying at least one voltage level to a plurality of subsystems on an integrated circuit having a system on chip (SOC) design, each of the subsystems having a plurality of units, at least two of the units located in at least one of the subsystems being different from each other, the DC voltage generator system comprising:

a plurality of local DC voltage generators distributed throughout the SOC chip, each local DC voltage generator independently supplying voltage to at least one unit of the plurality of subsystems, each local DC voltage generator including:

at least one regulator system incorporated in the local DC voltage generator, a power control unit and a clock control unit, wherein each local DC voltage generator receives a power control signal from said power control unit and a clock control signal from said clock control unit;

an AND gate receiving said power control signal and clock control signal and outputting a control signal;

a first transistor connected to the AND gate and controlled by said control signal;

a second transistor and a third transistor connected in series, the series connected at one end to a voltage source and to the other end to the first transistor for generating ~~and generates~~ a reference voltage;[[,]]

said at least one regulator system receiving said reference voltage and outputting a pump control signal, the pump control signal being enabled and disabled in response to at least the clock control signal; and

a pump system receiving the pump control signal and outputting the at least one voltage level in accordance with the pump control signal.

2. (Previously Presented) The DC voltage generator system according to Claim 1, wherein each local DC voltage generator is located proximate to a unit of the plurality of units.

3. (Previously Presented) The DC voltage generator system according to Claim 1, wherein each local DC voltage generator supplies the voltage level to one unit of the plurality of units.

4. (Previously Presented) The DC voltage generator system according to Claim 1, wherein a voltage level of the voltage supplied is selectable.

5. (Previously Presented) The DC voltage generator system according to Claim 1, wherein each local DC voltage generator is independently controlled by a respective control signal.

6. (Previously Presented) The DC voltage generator system according to Claim 5, wherein each respective control signal is generated by a power control unit in accordance with a power level mode at which the integrated circuit is operating.

7. (Previously Presented) The DC voltage generator system according to Claim 6, wherein the power control unit receives instructions from an external source for determining the power level mode.

8. (Previously Presented) The DC voltage generator system according to Claim 5, wherein each respective control signal is generated by a clock control unit.

9. (Previously Presented) The DC voltage generator system according to Claim 5, wherein each respective control signal is generated in accordance with an activity level of the SOC chip.

10. (Previously Presented) The DC voltage generator system according to Claim 9, wherein the activity level is one of a switching activity level and an I/O activity level.

11. (Previously Presented) The DC voltage generator system according to Claim 8, wherein the respective control signal controlling one of the local DC voltage generators is provided to the unit associated with the local DC voltage generator.

12. (Original) The voltage generator system according to Claim 5, wherein each respective control signal controls current flow in the local DC voltage generator.

13. - 21. (Cancelled)

22. (Previously Presented) The DC voltage generator system of Claim 1, further including a logic gate for simultaneously receiving the power control signal and the clock control signal and outputting a first signal for controlling the reference voltage.

23. (Currently Amended) A DC voltage generator system for supplying at least one voltage level to a plurality of subsystems on an integrated circuit having a system on chip (SOC) design, each of the subsystems having a plurality of units, at least two of the units located in at least one of the subsystems being different from each other, the DC voltage generator system comprising:

a power control unit for providing a corresponding power control signal to each of the plurality of units;

a clock control unit for providing a corresponding clock signal to at least each of the plurality of units;

a plurality of local DC voltage generators for independently supplying voltage to at least each of the plurality of units, each of the local DC voltage generators being located in a different

unit of plurality of units and including:

at least one regulator system, wherein each local DC voltage generator receives a corresponding power control signal from said power control unit and a corresponding clock control signal from said clock control unit;

an AND gate receiving said power control signal and clock control signal and outputting a control signal;

a first transistor connected to the AND gate and controlled by said control signal;

a second transistor and a third transistor connected in series, the series connected at one end to a voltage source and to the other end to the first transistor for generating ~~and generates~~ a reference voltage; ~~based on a supply voltage using a plurality of diodes,~~

said at least one regulator system receiving said reference voltage and outputting a pump control signal in accordance with said reference voltage, the pump control signal being enabled and disabled in response to at least the corresponding clock control signal; and

a pump system for receiving the pump control signal and outputting the at least one voltage level in accordance with the pump control signal.

24. (Previously Presented) The DC voltage generator system of Claim 22, further including a logic gate for simultaneously receiving the power control signal and the clock control signal and outputting a first signal for controlling the reference voltage.